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GIGABIT OPTICAL INTERCONNECTS: SYSTEM AND COMPONENT ANALYSIS, DESIGN AND DEVELOPMENT

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13. ABSTRACT (Maximum 200 words)

This report describes the results of experiments performed in various areas of technology required to develop gigabit optical interconnects for communication at 1.3um wavelength. First, we will summarize the analysis of optical correlation switches (i.e. optical "AND" gates) for use in time-division optical interconnects. Next, we describe the design and characterization of an all-optical, 30db contrast ratio GaAlInAs multiple quantum well asymmetric reflection modulator. Then, we comment on the characterization of polarization-dependent, strained-layer InGaAs/GaAs materials useful for light emitters and modulators. Finally, we report on the development of an optically transparent ATM packet switch testbed operating at 1.24416 Gbit/s. This work is a continuation of in-house efforts begun under 62702F, JON 4600P201 and summarized in RL-TR-91-398.

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1. Introduction

Optical interconnects are a means of alleviating the electronic input/output (I/O) bottleneck inherent in ultra-fast communication systems.[1] With the development of multi-gigahertz bandwidth optical interconnects as our goal, we have undertaken efforts to develop testbed architectures which demonstrate the physical-layer requirements of ultra-fast communication systems. These interconnect testbeds allow the study of current optical and electronic technology in an operational environment. As a result, testbed characterization and performance analysis of these off-the-shelf components have identified some deficiencies associated with their application in gigabit optical interconnects. Thus, development of materials and components which overcome these performance deficiencies is an ongoing major thrust of our experimental work.

The work performed in the current work unit can be summarized by four major efforts as follows.

1. Bit error rate (BER) and noise analysis of a photoconductive switch for use in time-division multiple-access interconnects.
2. Development of an all-optical, 30 dB contrast ratio GaAlInAs asymmetric reflection modulator.
3. Electro-optic characterization of InGaAs strained-layer materials for use as optical modulators.
4. Development of an optically transparent asynchronous transfer mode (ATM) packet switch operating at 1.24416 Gbit/s recognition rates.

Each of these efforts has resulted in a significant contribution to the development and design of multi-gigabit per second optical interconnects. It is also interesting to note that these components, analysis and architectures are not limited solely toward application in time-division-multiplexed, optical fiber interconnects. Indeed, many of the results reported here are applicable to free-space interconnects as well.

2. BER and Noise Analysis of a Photoconductive Switch

Optical time-division multiple-access (TDMA) and packet switch architectures have become an important means of implementing high-speed multi-user interconnects for local area and micro area networks.[2, 3] TDMA architectures utilize optical delays to time-division multiplex many data channels on a shared transmission medium, while packet switched architectures route frames of information from many data channels through a switching fabric. Both architectures operate with multiple gigabit per second (Gb/s) aggregate data rates. To eliminate the need for gigahertz bandwidth electronic processing in these architectures, the optical correlation function at the receiver must be carried out at the aggregate data rate of the interconnect system. For example, in a TDMA interconnect, demultiplexing is required to extract the baseband data from the high bit-rate time-multiplexed data. This function is performed using optical correlation, *i.e.* a logical AND operation, between the system clock and the multiplexed data. A similar correlation function is required in packet switched systems for the purpose of address recognition and routing control. Ideally, in both of these cases, the optical correlation processor allows the electronic processors to run at the baseband or frame rate of the system.

Many devices have been developed to perform this optical correlation function. Of these, photoconductive gates are of high interest due to their high speed/low noise characteristics as well as their ability to significantly reduce the complexity of the demultiplexing receiver circuitry.[3] However, these gates can impact bit-error-rate (BER) performance in a systems application due to limitations associated with sensitivity and contrast ratio. In this paper, we present the first analysis of the effects of the photoconductive gate contrast ratio and laser relative intensity noise (RIN) on the BER performance of multi-gigabit per second optical time-division applications. A detailed noise analysis indicates that laser RIN dominates the noise sources in a photoconductive gate. Example BER calculations for various values of contrast ratio and RIN are then undertaken to evaluate the performance of a photoconductive gate in an optical time-division application.

2.1 BER Development

For the development of this BER model, the electronic receiver is assumed to be an integrate-and-dump architecture where the integration interval can be varied over an integer number of received bits or channels. In a system implementation, this implies that the integration time can be a minimum of a bit length to a maximum of the frame length. The optical correlation detector is characterized by its noise properties, sensitivity, and on/off contrast ratio. The operating speed of the detector is taken into consideration by the number of bits over which the receiver is integrating. As a result, the development of the BER expression is valid for any data rate as long as the components characteristics such as operating bandwidth and noise expressions are valid at the assumed speeds. Finally, Gaussian statistics are assumed throughout the analysis since the sensitivity of optical correlation detectors is typically in the hundreds of femtojoule regime[4], *i.e.* approximately 4 x 10^6 photons/bit for InGaAs photoconductors.

Extending the analysis of Devetsikiotis, *et al.*,[5] the following expression for the BER of an optical time division receiver has been developed,

$$P_e = \sum_{n=0}^{N-1} \frac{(N-1)!}{n!(N-1-n)!} \left(\frac{1}{2}\right)^{N-1} \left[\operatorname{erfc}\left(\frac{\langle v_{1n} \rangle - v_T}{\sqrt{2}\,\sigma_{1n}} \right) + \operatorname{erfc}\left(\frac{v_T - \langle v_{0n} \rangle}{\sqrt{2}\,\sigma_{0n}} \right) \right] \qquad (1)$$

In Eq. (1), N is the number of bits (or channels) in the integration interval and n is the number of channels other than the correlated channel transmitting 1's within the integration interval. It should be noted that it has been assumed that a correlated 0 bit will generate the same signal level as an uncorrelated 1 bit. The first term in Eq. (1) is the probability that n 1's will be present in the integration interval, where the factor of 1/2 accounts for the probability of either a 1 or 0 being transmitted. The terms $\langle v_{in} \rangle$, where i = 1 or 0, are the mean signal voltages at the output of the

integrator when either a single 1 or single 0 is received. As a result, the received 1 and 0 signal levels have the form,

$$\langle v_{1n} \rangle = \langle v_1 \rangle + n\langle v_0 \rangle \qquad \text{and} \qquad \langle v_{0n} \rangle = (n+1)\langle v_0 \rangle \tag{2}$$

where $\langle v_1 \rangle$ is the mean signal of a 1 in one bit interval and $\langle v_0 \rangle$ is the mean signal of a 0 in one bit interval. The threshold voltage v_T is defined as,

$$v_T = \frac{\langle v_{10} \rangle + \langle v_{0(N-1)} \rangle}{2} \tag{3}$$

where $\langle v_{10} \rangle$ is the lowest possible mean signal when a 1 is received and $\langle v_{0(N-1)} \rangle$ is the highest possible mean signal when a 0 is received. As is evident from Eqs. (2) and (3) as n increases toward large N, the BER is greatly dependent on the contrast ratio $\kappa = \langle v_1 \rangle / \langle v_0 \rangle$. The σ_{in} terms are the rms noise voltages at the output of the integrator,

$$\sigma_{1n} = \sqrt{\langle \sigma_1^2 \rangle + n\langle \sigma_0^2 \rangle} \qquad \text{and} \qquad \sigma_{0n} = \sqrt{(n+1)\langle \sigma_0^2 \rangle} \tag{4}$$

where $\langle \sigma_1^2 \rangle$ and $\langle \sigma_0^2 \rangle$ are the mean-squared noise voltages for a received 1 and 0 in one bit period, respectively.

2.2 Noise Analysis

The BER performance of the receiver depends not only on the contrast ratio of the photoconductive gate, but also on the noise in the photoconductor, the subsequent electronic circuitry, and the laser transmitter. The dependence on noise associated with the laser transmitter can be greatly reduced by increasing the sensitivity of the photodetector. Since typical photoconductors have sensitivities on the order of hundreds of femtojoules, the laser RIN can not

be neglected. An equivalent circuit for the receiver based on a mean-squared noise current generator $\langle i_N^2 \rangle$ is shown in Figure 1 and given as,[6]

$$\langle i_N^2 \rangle = 4e\Delta f\left(\frac{\tau_o}{\tau_d}\right)\left[\frac{\langle i_s \rangle + i_d}{1 + 4\pi^2\tau_o^2 f^2}\right] + \frac{4kT\Delta f}{R_g} + \left(\frac{e\eta P_0}{h\nu}\right)^2 (RIN)\Delta f \qquad (5)$$

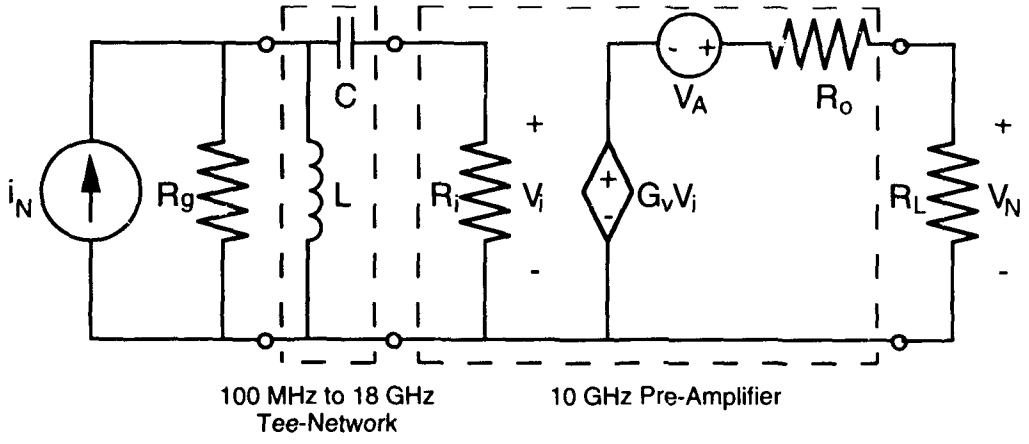


Figure 1 Equivalent circuit model of the photoconductive AND gate used for the noise and BER analysis.

In this equation, the first term is the generation-recombination noise where τ_o is the hole lifetime (8 ps) and τ_d is the electron transit time across the photoconductive gap (42 ps), e is the electron charge (1.6022×10^{-19} C), Δf is the circuit bandwidth (9.9 GHz), $\langle i_s \rangle$ is the mean signal current in one bit-interval (312.8 μA), i_d is the gate dc dark current (160 μA) and f is the signal frequency (100 MHz). The second term is the thermal noise where k is Boltzmann's constant (1.381×10^{-23} J/K), T is room temperature (290K) and R_g is the gate dark resistance (19kΩ). The third term is the relative intensity noise of the source laser where η is the quantum efficiency (0.56), P_0 is the incident power per bit (10.86 mW, *i.e.* a bit energy of 2.2 pJ), hν is the energy per photon (1.524×10^{-19} J at 1.3 μm) and RIN is the relative intensity noise. In typical receiver circuitry, the gate is

ac-coupled to the pre-amplifier by a tee-network as shown in the equivalent circuit. Due to the band-pass characteristic of the tee-network, the low frequency noise, *i.e.* below f, of the photoconductive gate is neglected in the noise analysis. The amplifier noise contribution is modeled as a noise voltage source at the output of the amplifier in Figure 1. The amplifier mean-squared noise voltage is given by the expression,

$$\langle v_A^2 \rangle = 4\,k\,(F - 1)\,T\,\Delta f\,R_i \tag{6}$$

where F is the amplifier noise figure (F = 5) and R_i is the amplifier input impedance (50 Ω). The mean-squared noise voltage across the load resistor R_L is given by

$$\langle v_N^2 \rangle = \left(\frac{1}{2}\right)^2 \left[\langle v_A^2 \rangle + \left[\frac{G_v R_g R_i}{R_g + R_i} \right]^2 \langle i_N^2 \rangle \right] \tag{7}$$

where G_v is the amplifier voltage gain (G_v = 5). Eq. (7) is used to evaluate Eq. (4), *i.e.* $\langle \sigma_i^2 \rangle = \langle v_N^2 \rangle$.

The values of the parameters given for these noise equations have been measured or calculated for an InGaAs photoconductive gate[7] similar to that reported by Desurvire, *et al.*[4] Using Equations (5), (6) and (7) and a typical value of -145 dB/Hz for the RIN of semiconductor lasers,[8, 9] the noise power for the thermal, generation-recombination, amplifier, and relative intensity noise sources at the output of the amplifier are calculated to be -85.9 dBm, -67.5 dBm, -68.0 dBm, and -34.0 dBm respectively. From these values, it is clear that the photoconductive gate and receiver circuit is very low noise and that the noise in the received signal will be dominated by the RIN of the laser.

2.3 BER Performance

Utilizing the results of the noise analysis, the BER performance of the InGaAs photoconductive gate in a time-division application can be estimated. In the calculations a value of

78.2 mV for the mean signal voltage $\langle v_1 \rangle$ is used[7] and $\langle v_0 \rangle$ is calculated for a given contrast ratio κ. BER calculations using Eq. (1) are then performed as a function of the number of bits (or channels) in the integration interval N for various values of contrast ratio κ and laser RIN. Figure 2 presents the results for contrast ratios of 10, 20 and 30 dB and laser RINs of -143 dB/Hz and -146.3 dB/Hz.

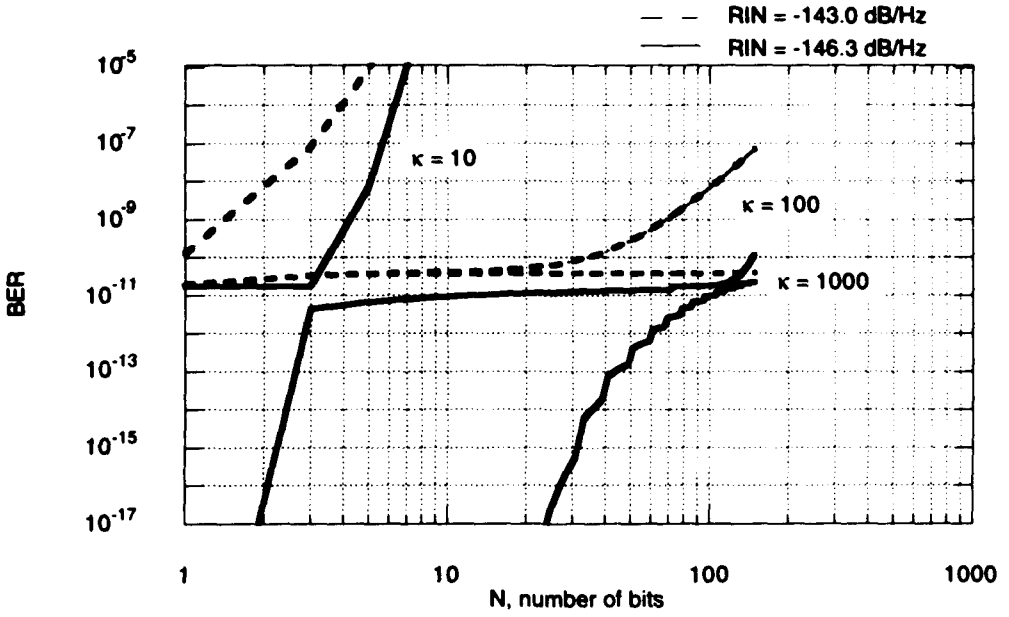


Figure 2 Calculated BER as a function of the number of bits in the integration interval N for κ = 10, 100, and 1000 and a laser RIN of -143 dB/Hz (solid lines) and -146.3 dB/Hz (dashed lines).

As shown in the figure, for a RIN of -143 dB/Hz, to achieve less than a 10^{-9} BER, $\kappa = 10$ allows for integration over only one bit beyond the correlated channel, while increasing the contrast ratio to $\kappa = 100$ allows for integration over 55 bits. Further increasing κ to 1000 allows for integration over more than 1000 bits. For a reduction in laser RIN of just over 3 dB to a value of

-146.3 dB/Hz, a dramatic effect on the calculated BER is observed. To achieve a BER of less than 10^{-9}, $\kappa = 10$ allows for integration over 4 bits, while integration over more than 160 bits is allowed for $\kappa = 100$. It is interesting to note that most of these values of κ and RIN do not allow for a BER of less than 10^{-15}, a value which may be required in gigahertz bandwidth communication systems. To achieve a BER of less than 10^{-15}, a RIN of -146.3 dB/Hz and $\kappa = 100$ allows for integration over only two bits, while an increase of the contrast ratio to $\kappa = 1000$ increases the integration interval to just over 31 bits. This result emphasizes the dependence of the BER on noise in the received signal. In fact, a further reduction of laser RIN to a value of -150 dB/Hz results in a BER of $< 10^{-15}$ with the ability to integrate over 3, 73 and >1000 bits for $\kappa = 10$, 100 and 1000, respectively.

The BER performance of an InGaAs photoconductive gate has been investigated for time-division applications for the first time. The contrast ratio and sensitivity of the photoconductive gate are shown to greatly affect the bandwidth of the receiver electronics required to process the detected signal, *i.e.* the number of bits the receiver can integrate over while maintaining the BER performance of the application. As a result, improvements in photoconductive gate and semiconductor laser characteristics are needed for the use of such components in practical time-division interconnect systems. Further reductions in laser RIN characteristics may not easily be achieved. However, increased detector sensitivity reduces the requirement of large bit energies, thus reducing the effect of laser RIN on receiver BER performance. Low-temperature molecular beam epitaxy grown materials for photoconductive devices already show promise in the areas of increased contrast ratio and sensitivity while operating at multi-hundred gigahertz frequencies.[10]

3. All-Optical, High Contrast Asymmetric Reflection Modulator

As indicated in Section 2 of this report, high contrast optical devices are essential elements for fully utilizing the bandwidth available in optical interconnects. Semiconductor multiple quantum well materials have shown great promise in achieving this result. Indeed, we have developed an optically-controlled, high contrast modulator for use in the technologically important 1.3 μm wavelength region[11]. The device is a GaAlInAs/AlInAs multiple quantum well asymmetric Fabry-Perot reflection modulator. The modulator takes advantage of the large absorptive and refractive nonlinearities associated with saturating the heavy-hole exiton resonance. These effects coupled with the Fabry-Perot configuration result in on/off contrast ratios exceeding 30 dB and an insertion loss of less than 2.2 dB at a low pump intensity of 30 kW/cm^2.

Because of the reflective nature of this type of device, use in free space as well as optical fiber interconnects is intended. The speed of the device was found to be limited to on the order of 1 GHz due to the measured recovery time of approximately 725 ps. This recovery time is consistent with past measurements of carrier lifetimes in similar materials[12]. For this reason, the device would be most useful as an off-chip modulator in a multi-gigabit per second interconnect. However, the device can also be used as a demultiplexer or gating switch in lower aggregate bandwidth systems such as would be necessary for packet switching.

4. Electro-Optic Strained-Layer Multiple Quantum Well Modulators

Electro-optic modulators are a necessary component of emerging optical fiber based local area interconnects. The electro-optic version of the all-optical asymmetric Fabry-Perot reflection modulator (ARM) of Section 3 and completed under this work is more fully described elsewhere[13]. However, a brief summary of the experimental work is given here. This type of an intensity modulator uses an electro-optic material as the spacer material to balance the normally

unequal front and back mirror reflectances. The quantum confined Franz-Keldysh and Stark effects shift the absorption edge of semiconductor multiple quantum well (MQW) materials to longer wavelengths in the presence of an external electric field applied perpendicular to the MQW layers, thereby changing the reflectance of the etalon. The combined coherence effects of the etalon coupled with the quantum effects of the MQW materials result in a large modulation depth and a low insertion loss.

P-I-N diode structures using an $In_{.16}Ga_{.84}As/GaAs$ MQW structure as the intrinsic region were fabricated for the purpose of characterizing the electroabsorption associated with different applied electric fields. Quantum confined Franz-Keldysh and Stark shifts were observed for applied electric fields as large as 6.58×10^4 V/cm. The resulting change in the absorption coefficient was found to be -3.7×10^3 cm^{-1} which is sufficient to design a high-speed ARM with a large modulation depth and a low insertion loss.

Further electroabsorption characterization of InGaAs/Gas structures oriented in the [100] crystallographic direction resulted in the observation of polarization-dependent effects[14]. These results demonstrate that it is possible to build a polarization-sensitive electroabsorption device. This type of device would find particular use with vertical cavity surface emitting lasers. A reprint of the published result follows.

5. Optically Transparent Asynchronous Transfer Mode Packet Switch Node

Packet switching technology is emerging as a means of routing very high bit rate, bursty data traffic. Much work has been developed in the area of interconnects which involve optical to electronic to optical conversion of the signal, such as SONET and FDDI token ring systems. However, in order to avoid the electronic bottleneck inherent in multi-gigabit systems, all-optical approaches must be developed. Traditionally, these interconnects incorporate electro-optic control of an optically transparent path. Thus, most work has been dedicated to developing an efficient

means of header transmission/detection for packet routing. These include subcarrier multiplexed [15] and bit per wavelength [16] techniques. The subcarrier multiplexed technique requires that the data payload has a bandwidth lower than that of the subcarrier and may be difficult to implement at very high bit rates as well as increase the latency encountered in a packet traversing a large interconnect. The bit per wavelength technique is limited by the inherent dispersion of the packet since each bit in the packet is of a different wavelength as well as very costly in terms of the number of transmitters and receivers required per node. On the other hand, traditional serial intensity-modulated direct-detection (IM-DD) signals have been shown to be adequate at very high data rates [17].

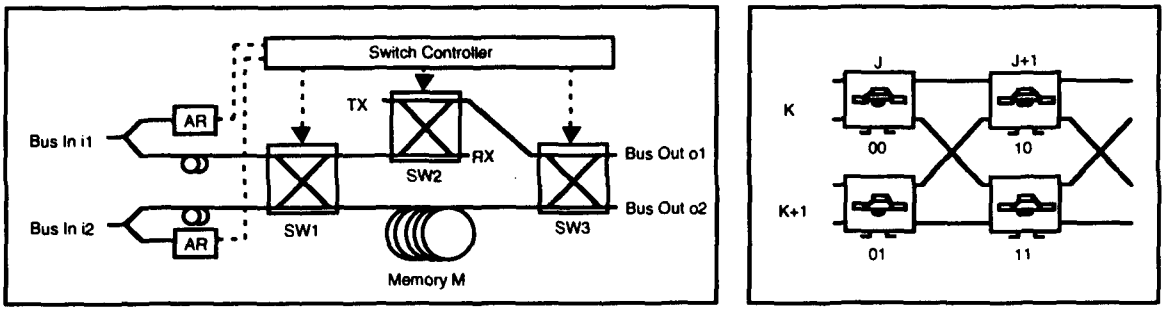
Multihop packet switching networks with regular two-connected topologies have been proposed for all-optical implementation at very high bit rates. We have developed a novel optically transparent packet switch node structure for use in just such a two-connected, slotted network. The node performs the functions of routing, buffering and drop/add multiplexing. The node is self-clocked at an address recognition rate of 1.24416 gigabit per second, using IM-DD signals. A brief description of the experimental results follows[18].

Extremely high bit rates can be used in transmission by each node in space switching transparent optical networks, since nodes are connected by dedicated fiber links. The electronic control of the switching nodes may limit the bit rate since routing computations must be performed within a packet's duration. Extremely simple node structures are thus desirable that have low loss and simple control, while still providing good throughput-delay performance.

5.1 Theory

A new node structure shown in Figure 3a with a single transmitter TX and receiver RX employing deflection routing [19] is proposed here for two-connected, slotted networks. Only three 2x2 optical switches are used, the theoretical minimum of all possible single-buffer all-optical

node schemes, for a node capable of accessing/receiving either channel. Without the one-packet fiber delay loop memory M [20], it would be a 3x3 completely non-blocking switch.



a) b)

Figure 3. a) Schematic diagram of transparent optical node. b) Node configuration for routing experiment.

Packets entering the node at i1 or i2 and contained in M are perceived by the controller in one of five possible ways: empty (E), for the node (FN), caring to exit on output o1 (C1), caring to exit on output o2 (C2), or don't care (DC), i.e., both outputs provide equivalent shortest-paths to their destination. Deflections occur when packets at the input of SW3 vie for the same output. When i1 and i2 are FN, one is missed. The objective of the controller is to maximize the node's throughput by minimizing the number of deflections. Switch SW2 is just for absorption/injection, and routing switch SW3 is controlled with a simple non-priority hot-potato routing [19] of its input packets. The description of the switch settings ("i?" stands for "one of the two inputs") is as follows:

if (i1=i2) ⇒ Randomize SW1

elseif (i?=FN) ⇒ set SW1 to receive it

elseif ((i1,i2)=C1,C2) or (C2,C1)) and (M=E or DC) ⇒ Randomize SW1

elseif (i?=E) and (TX=full) ⇒ set SW1 to receive E

elseif (M,i?) = ((C2,C2) or (C1,C1)) ⇒ store that input

else store E's or DC's

Absorption of FN packets is done first. Line 3 accounts for the fact that two care non-conflicting packets cannot be routed out directly, as memory cannot be bypassed. Emp' are routed to TX for possible injection. Conflicts with the memory are resolved by sto..g the conflicting input. E's and DC's are stored when possible to avoid deflections at the next slot.

The throughput vs. offered load (i.e., the probability of having a packet ready at TX at each clock) for a 64-node ShuffleNet in uniform traffic has been theoretically evaluated [21]. I comparison with the throughput of nodes with no delay loop memory M (i.e., hot-potato routing) and of nodes with infinite-buffers (i.e., store-and-forward S&F) at full load, the proposed node structure yields 71% of the maximum S&F throughput while the node with no delay loop memory yields only 52%. This is a 37% increase in throughput at the cost of building only a slightly more complicated controller.

5.2 Experiment

The transparent optical node illustrated in Figure 3a was constructed with three Crystal Technology SW313P $LiNbO_3$ electro-optic crossbar switches (SW1, SW2 and SW3) and a length of optical fiber for the purposes of routing, buffering and drop/add multiplexing of incoming packets. The $LiNbO_3$ switches were measured to have average fiber-to-fiber losses of -6.4 dB when connected in the configuration of Figure 3a for an overall throughput loss of -19.2 dB for a

packet traversing all three switches. Such a loss can be reduced by 3 to 6 dB by improving the fiber splice connections within the node structure. Power levels can be restored using an optical amplifier placed at the bus output ports of the node. However, the noise introduced by optical amplifiers imposes an upper limit on the maximum usable bit rate [22]. For these experiments a four node banyan interconnect as shown in Figure 3b was assumed for routing purposes. Th:·· valid binary packet destination addresses JK for this interconnect are 00, 01, 10 and 11.

Address recognition is performed at input port i1 by tapping off a portion of the incoming signal power with a -3 dB splitter and detecting the address signals of interest. The power in the address recognition portion of the signal is sent through an optical fiber 1x4 divider and delay structure for parallel detection of four bits of information in the packet header field. ATM packet structures consisting of a 5 byte header field and 48 byte data field were used. A portion of a typical 1.24416 Gbit/s NRZ input packet is shown in Figure 4. These data are optical pulses detected with an AT&T 127B InGaAs avalanche photodiode and measured with a Tektronix 11801 digitizing sampling oscilloscope and an SD-26, 20 GHz bandwidth sampling head.

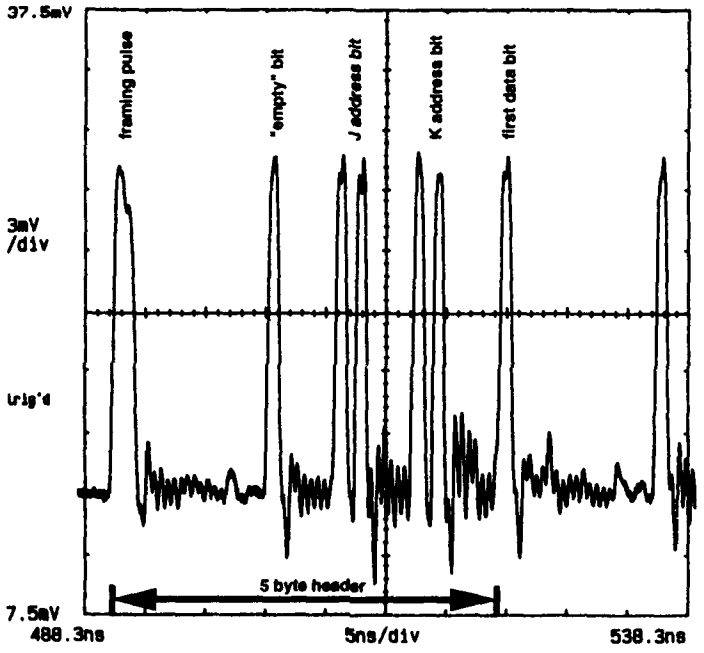


Figure 4. Detected header field of a typical packet.

Every incoming packet structure, including empty packets, begins with a two-bit-wide framing pulse in the header field. The framing pulse is used for self-clocking of packets entering the node and to maintain overall network synchronization. Since the framing pulse must be sent with every packet time slot, an address bit E in the header field is used to determine whether or not an empty packet has been sent in the slot. When the destination address bits J or K had digital values of zero they were always surrounded by optical one bits to ensure that a true zero was detected at the 1.24416 Gbit/s data rate. Prior to entering the node, the packet is buffered by a length of optical fiber while the state of the three $LiNbO_3$ switches is set according to the prioritization algorithm. This address recognition delay stage is 120 ns, 92 ns of which is due to propagation delays in the electronic controller circuitry. The majority of this time, approximately 83 ns, is associated with the setup and hold time requirements of a CMOS programmable logic array used to derive the switch state settings from 2^{14} possible input combinations. These controller inputs are the three-bit destination address information (EJK) of packets at i1, i2, TX and M, as well as the two bit address of the optical node itself.

Experimental results for the switch operating as node address 00 and with empty packets incident at TX are shown in Figures 5a and 5b. Figure 5a is a plot of the series of incoming packets at TX (upper trace), i1 (middle trace) and i2 (lower trace). The data rates for packets at i1 and i2 were 1.24416 Gbit/s and 622.08 Mbit/s, respectively, and have low mark ratios for viewing purposes. Indeed, the data rates in the packet data fields can be multi-Gbit/s. The guardband between packets is 51.44 ns. The empty packets incident at TX have no framing pulse associated with the packet time slot due to unavailability of a third modulatable laser source. The i2 packets all have the same destination address of 101. The packets incident at i1 have destination addresses 100, 110, 000 and 111, respectively. The packets detected at the output ports are shown in Figure 5b. The packet with destination address 100 is correctly dropped at RX (upper trace) followed by empty packets from TX, i1 and TX. Packets detected at o1 (middle trace) have destination address 101 from TX, 000 from M via i2, 110 from M via i1, and 000 from M via i2. Packets detected at

o2 (lower trace) have destination address 111 from M via i1, 101 from TX, 101 from TX and 101 from TX.

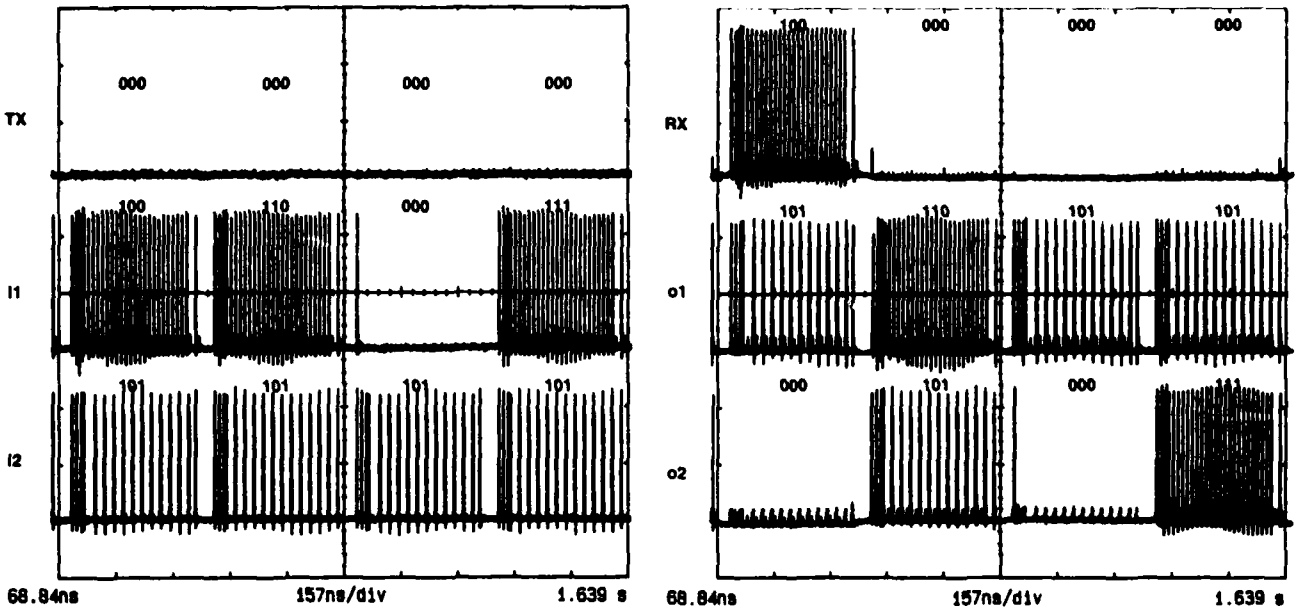


Figure 5. a) Incident packets at input ports TX (upper trace), i1 (middle trace) and i2 (lower trace) with respective destination addresses identified. b) Departing packets at output ports RX (upper trace), o1 (middle trace) and o2 (lower trace) with respective destination addresses identified.

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